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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/728,262	CHEN ET AL.
	Examiner	Art Unit
	Linh M. Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-15 and 17-19* is/are rejected.

7)☒ Claim(s) *10,16 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a reply to Applicants' amendment filed 03/18/200. By virtue of the amendment, claims 17-20 are newly added, thus claims 1-20 are currently presented in the instant application.

Claim Objections/Minor Informalities

1. Claim 19 is objected to because of the following informalities:

line 1, delete "is".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 and 11-15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro (U.S. Pat. No. 5,864,254) in view of Doblar et al. (U.S. Patent No. 6,640,309).

With respect to claim 1, Tashiro discloses, in Figs. 1 and 2A, a method for regenerating signals comprising converting signals [IN1, IN2] having either single-ended pulses or differential pulses into signals having substantially the same voltage swing [OUT].

Tashiro fails to explicitly disclose that the input signals are clock signals.

Doblar et al. discloses, in Fig. 3, a differential amplifier circuit with input signals as clock signals.

To configure the circuit of Tashiro with input signals as clock signals as taught by Doblar et al. for regenerating clock signals substantially at the same frequency would have been obvious to one of ordinary skill in the art at the time of the invention since Doblar et al. teaches that such by employing such circuit would facilitate synchronization *(see Doblar. et al., col. 2, lines 17-26)*.

With respect to claim 2, the combined teaching of Tashiro and Doblar et al. discloses, col. 5, lines 13-39 and col. 7, lines 4-15, that the single-ended clock pulses are provided by a TTL logic circuit and wherein the differential clock pulses are produced by an ECL logic circuit.

With respect to claim 3, Tashiro discloses, in Figs. 1 and 2A, a method for regenerating signals comprising providing a source of signals, such source producing either single-ended pulses or differential pulses [IN1, IN2], such signals being fed to a regeneration circuit, such regeneration circuit converting such clock signals having either the single-ended clock pulses or the differential pulses into signals having substantially the same voltage swing [OUT].

Tashiro fails to explicitly disclose that the input signals are clock signals.

Doblar et al. discloses, in Fig. 3, a differential amplifier circuit with input signals as clock signals.

To configure the circuit of Tashiro with input signals as clock signals as taught by Doblar et al. for regenerating clock signals substantially at the same frequency would have been obvious to one of ordinary skill in the art at the time of the invention since Doblar et al. teaches that such by employing such circuit would facilitate synchronization *(see Doblar. et al., col. 2, lines 17-26)*.

With respect to claim 4, Tashiro discloses, in Figs. 1 and 2A, a regeneration circuit comprising a) a differential amplifier [1] having a non-inverting input terminal and an inverting input terminal; b) a first voltage divider network [R3, R4] coupled between a pair of reference voltages [VDD and GND] and the non-inverting input terminal; c) a second voltage divider network [R3, R4] coupled between the pair of reference voltages and the inverting input terminal; wherein the first and second voltage divider networks produce the same differential voltage swing for both single-ended or differential source signals voltage at the inverting and non-inverting input terminals.

Tashiro fails to explicitly disclose that the input signals are clock signals.

Doblar et al. discloses, in Fig. 3, a differential amplifier circuit with input signals as clock signals.

To configure the circuit of Tashiro with input signals as clock signals as taught by Doblar et al. for regenerating clock signals substantially at the same frequency would have been obvious to one of ordinary skill in the art at the time of the invention since Doblar et al. teaches that such by employing such circuit would facilitate synchronization *(see Doblar. et al., col. 2, lines 17-26)*.

With respect to claim 5, the combined teaching of Tashiro and Doblar et al. discloses that the first voltage divider network [R3, R4] includes a pair of resistors, a first one of the pair of resistors, R1, being connected between a first one of the pair of reference voltages and the non-inverting input and a second one of the pair of resisters, R2, being connected between the non-inverting input and the second one of the pair of reference voltages.

With respect to claim 6, the combined teaching of Tashiro and Doblar et al. discloses that the second voltage divider network [R3, R4] includes a pair of resistors, a first one of the pair of resistors, R3, being connected between a first one of the pair of reference voltages and the inverting input and a second one of the pair of resisters, R4, being connected between the inverting input and the second one of the pair of reference voltages.

With respect to claim 7, the combined teaching of Tashiro and Doblar et al. discloses that R1 is has the same resistance as R3 and R2 has the same resistance as resistor R4.

With respect to claim 8, Tashiro discloses, in Figs. 1 and 2A, a regeneration circuit comprising a) a differential amplifier [1] having a non-inverting input terminal and an inverting input terminal; b) a first voltage divider network [R3, R4] coupled between a pair of reference voltages [VDD and GND] and the non-inverting input terminal; c) a second voltage divider network [R3, R4] coupled between the pair of reference voltages and the inverting input terminal; wherein the first and second voltage divider networks produce the same differential voltage swing for both single-ended or differential source signals voltage at the inverting and non-inverting input terminals.

Tashiro fails to explicitly disclose that a) the input signals are clock signals and b) a transmission line coupled between a source of clock signals and the input terminals, and wherein such transmission line has a characteristic impedance Zo, and wherein R1*R2/(R1+R2) equals Zo.

Doblar et al. discloses, in Fig. 3, a) a differential amplifier circuit with input signals as clock signals and b) transmission line impedance [col. 6, lines1-3].

To configure the circuit of Tashiro with input signals as clock signals as taught by Doblar et al. for regenerating clock signals substantially at the same frequency and for having the same characteristic impedance *(base on the same structure)* would have been obvious to one of ordinary skill in the art at the time of the invention since Doblar et al. teaches that such by employing such circuit would facilitate synchronization *(see Doblar. et al., col. 2, lines 17-26)* and furthermore it would have been obvious to one of ordinary skill in the art at the time of the invention to configure the circuit with impedance matching for the transmission lines in order to prevent signal reflection within the transmission lines *(similar structure yields similar characteristic impedance)*.

With respect to claim 9, the combined teaching of Tashiro and Doblar et al. discloses that the potential difference provided by the pair of reference voltages voltage, Vcc [VDD], times (R2/(R1+R2)) and Vcc, times (R3/(R3+R4)) are selected to provide predetermined proper terminating voltages to the emitter coupled logic circuit *(col. 6, lines 3-6, that "ECL circuits is highly desirable in clock signal distribution circuits")*.

With respect to claim 11, Tashiro discloses, in Figs. 1 and 2A, a method for regenerating signals comprising a) providing a pulse regeneration circuit; and b) feeding to signals to the regeneration circuit, such regeneration circuit converting such clock signals having either the single-ended pulses or the differential clock pulses into signals having substantially the same voltage swing; providing such regeneration circuit with a differential amplifier [1] having a non-inverting input terminal and an inverting input terminal; a first voltage divider network [R3, R4] coupled between a pair of reference voltages and the non-inverting input terminal; a second voltage divider network [R3, R4] coupled between the pair of reference voltages and the

inverting input terminal; wherein the first and second voltage divider networks produce the same voltage at the inverting and non-inverting input terminals.

Tashiro fails to explicitly disclose that the input signals are clock signals and the step of providing a source of clock signals, such source of an ECL logic circuit for producing differential clock pulses.

Doblar et al. discloses, in Fig. 3, a differential amplifier circuit with input signals as clock signals and in col. 6, lines 3-6, that "ECL circuits is highly desirable in clock signal distribution circuits".

To configure the circuit of Tashiro with input signals as clock signals as taught by Doblar et al. for regenerating clock signals substantially at the same frequency would have been obvious to one of ordinary skill in the art at the time of the invention since Doblar et al. teaches that such by employing such circuit would facilitate synchronization *(see Doblar. et al., col. 2, lines 17-26).*

With respect to claim 12, the combined teaching of Tashiro and Doblar et al. discloses that the first voltage divider network [R3, R4] includes a pair of resistors, a first one of the pair of resistors, R1, being connected between a first one of the pair of reference voltages and the non-inverting input and a second one of the pair of resisters, R2, being connected between the non-inverting input and the second one of the pair of reference voltages.

With respect to claim 13, the combined teaching of Tashiro and Doblar et al. discloses that the second voltage divider network [R3, R4] includes a pair of resistors, a first one of the pair of resistors, R3, being connected between a first one of the pair of reference voltages and the

inverting input and a second one of the pair of resisters, R4, being connected between the inverting input and the second one of the pair of reference voltages.

With respect to claim 14, the combined teaching of Tashiro and Doblar et al. discloses that R1 is has the same resistance as R3 and R2 has the same resistance as resistor R4.

With respect to claim 15, the combined teaching of Tashiro and Doblar et al. discloses all the claimed limitations in claim 11-14 and transmission line impedance [col. 6, lines1-3] except for such transmission line has a characteristic impedance Zo, and wherein R1*R2/(R1+R2) equals Zo.

To configure the circuit of the combined teaching of Tashiro and Doblar et al. having transmission line impedance with impedance Zo, and wherein R1*R2/(R1+R2) equals Zo would have been obvious to one of ordinary skill in the art at the time of the invention since impedance matching for the transmission lines in order to prevent signal reflection within the transmission lines *(similar structure yields similar characteristic impedance).*

With respect to claim 17, the combined teaching of Tashiro and Doblar et al. discloses that the voltage divider network [R3, R4] includes a pair of resistors, a first one of the pair of resistors, R1, being connected between a first one of the pair of reference voltages and the non-inverting input and a second one of the pair of resisters, R2, being connected between the non-inverting input and the second one of the pair of reference voltages.

With respect to claim 18, the combined teaching of Tashiro and Doblar et al. discloses that the second voltage divider network includes a pair of resistors [R3, R4], a first one of the pair of resistors, R3, being connected between a first one of the pair of reference voltages and the

inverting input and a second one of le pair of resisters, R4, being connected between the inverting input and the second one of the pair of reference voltages.

With respect to claim 19, the combined teaching of Tashiro and Doblar et al. discloses that R1 has the same resistance as R3 and R2 has the same resistance as resistor R4.

Allowable Subject Matter

4. Claims 10, 16 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

A clock regeneration circuit, in which the source of clock pulses is a transistor-transistor logic circuit having an output transistor, such output transistor having an emitter and collector coupled between the pair of reference potentials, and including a coupling resistor R5 serially connected between the collector electrode and the non-inverting input though the transmission line, such resistor R5 being selected to provide a predetermined proper voltage swing across the non-inverting and inverting inputs, as called for in claim 10 or claim 16; and

A clock regeneration circuit, in which a resistor serially connected between a source of clock pulses and one of the input terminals of the differential amplifier, as called for in claim 20.

Remarks

5. Applicant's arguments with respect to claims 1-4, 8 and 11-15 have been considered but are moot in view of the new ground(s) of rejection.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGU
PRIMARY EXA